



### Overview:

The VXL Viterbi Decoder IP core implements the Viterbi algorithm for decoding a bitstream encoded by a corresponding Forward Error Correction convolutional encoding system. A lot of digital communication systems incorporate a Viterbi decoder for decoding convolutionally encoded data. By using the minimum likelihood algorithm, the Viterbi decoder core is able to correct errors in received data caused by channel noise. The decoded output data is equivalent to the transmitted digital data stream.

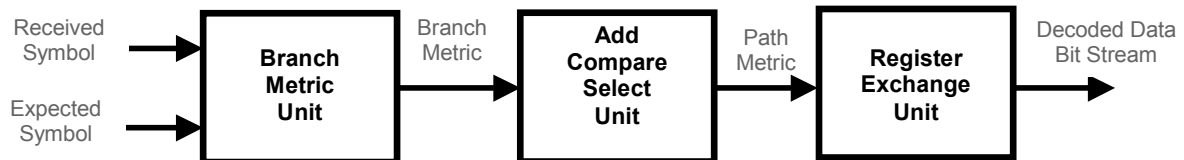
### Application:

- Industry standard constraint length 7, rate =  $\frac{1}{2}$ , (G0, G1) = (171, 133)
- High output data rates of up to 45 Mbps
- Low latency of 111 clocks.
- Parallel architecture design
- Trace-back logic for continuous decoding
- Trace back length of 35
- Soft decision decoding
- Fully synchronous design

### Key Benefits:

- Small silicon footprint
- High throughput/data rates
- Low latency
- Bit equivalent Matlab Model available
- Elaborate Test bench.
- Parameterizable HDL core design
- RTL source code available for easy integration and implementation

### Block diagram:



### Applications:

- Satellite communications
- Data storage devices
- Decoding Trellis-Coded Modulation (TCM) systems (telephone line modems, amateur radio, radio relay and satellite communications)

## Application Note – OFDM Receiver System:

The OFDM receiver system performs table look-ups and MAC intensive transform operations. The system supports variable data size (4 to 16 bits) and variable data rate (40 to 320 Mbps). Data are represented as real and complex values. The system supports 8-bit precision for input and output. The FIR unit is a 127-tap FIR filter with real coefficients and the FFT unit is a 256-point complex FFT. The Slicer block is a QAM-256 demapper. The final stage is the Viterbi Soft decision decoder.



### Deliverables:

- Core options
  - RTL design in VHDL
  - Technology specific netlist
- Bit equivalent Matlab model
- Test bench
- Documentation

### Target Technologies:

- FPGA: Spartan 3, Virtex, Virtex 2/Pro, Virtex 4, Virtex 5
- ASIC standard cell

### Device utilization summary:

Target Device	Max. Frequency (MHz)	Slices used	Block RAMs
Xilinx Virtex V600BG432-6	26	1991	5

**Think Silicon**  
VLSI Design & Consultancy

**Think Silicon Ltd.**  
Patras Science Park  
Rion Ahaias 26504  
Greece  
Tel: +30 2610 911543  
Fax: +30 2610 911543  
E-mail: [sales@think-silicon.com](mailto:sales@think-silicon.com)  
Web: <http://www.think-silicon.com>



This product was developed by the IP core experts at VXL Technologies Ltd.