

Overview:

The VXL parameterizable Reed-Solomon, RS (255, 239) IP core is optimized in terms of speed and area. The core is available for Xilinx Spartan and Virtex series FPGA's. ASIC standard cell libraries flow is also provided according to customer request.

Features:

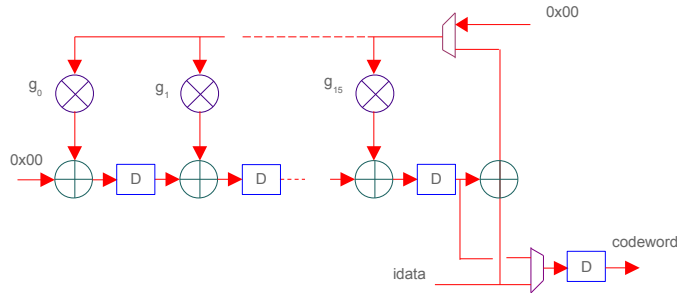
- Standard configuration RS(255, 239)
- OTN G.709 compliant implementation
- 255-symbol block size
- 8-bit symbol size
- Synchronous single clocked pipeline design
- Continuous data flow operation
- No gaps between code blocks
- Count of corrected error symbols (when less than or equal to 8)
- Detection of error symbols (when more that 8)

Key Benefits:

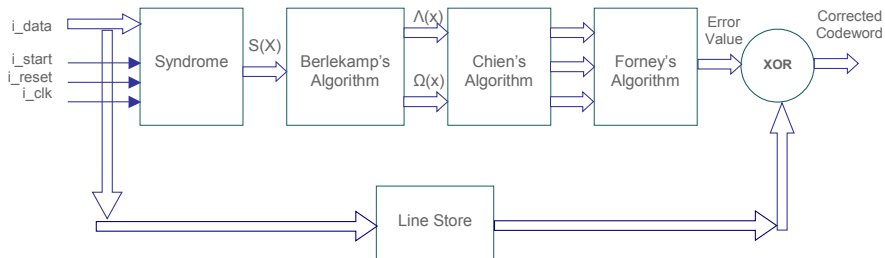
- Small silicon footprint
- High speed capabilities
- Easily modifiable to implement different Reed-Solomon coding standards
- Parameterizable design
- FPGA proven for Xilinx Virtex and Spartan series FPGA
- ASIC standard flow also supported according to customer needs.
- RTL source code available for easy integration and implementation

Block Diagram:

Encoder Architecture:

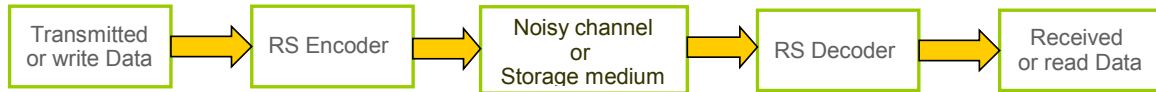


Decoder Architecture:



Applications:

- Forward Error Correction (FEC) codes
- Data Storage Systems
- Server Layer fo SDH, ATM, IP, Ethernet
- High speed fiber optic signals (40 Gbps and beyond)
- Data storage systems (CD, DVD codecs)
- Data transmission like DSL systems.
- Satellite communications



Deliverables:

- Code options
 - RTL design in VHDL
 - Technology specific netlist
- Test bench
- Documentation

Target Technologies:

- FPGA: Spartan 3, Virtex, Virtex 2/Pro, Virtex 4, Virtex 5
- ASIC standard cell

Device utilization summary:

Target Device	Max. Frequency (MHz)	Slices used	Block RAMs
Xilinx Virtex XC4VSX35-10-FF668	118	2567	4

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This product was developed
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