



VLSI Design & Consultancy

## **DATASHEET**

**JTAG IEEE1149.1 Generator  
Version 1.0**



## 1 Overview

The Think Silicon *JTAG 1149.1 Generator* is a configurable web based generator for JTAG wrapper for Semiconductor IC Devices.

## 2 Features

- Easy to use Graphical Web User Interface
- IEEE1149.1 compliant FSM
- Support for TRST and 5 sequential TMS for reset
- Support for User Configurable DEVICE ID code
- User configurable Boundary Scan Chain number and type of Cells (BC1,BC2, BC4, Three state pads)
- Boundary Scan Registers clocked on rising edges of generated TCK and TCKn.
- Supports EXTEST, IDCODE, BYPASS, SAMPLE, PRELOAD instructions

## 3 Architecture

### 3.1 Block Diagram

The Think Silicon *JTAG wrapper* consists of the following components:

- The TAP FSM. The TAP FSM is a hardware representation of the IEEE1149.1 Finite State Machine, where all state transitions are mapped in hardware. The TAP FSM Control logic extracts IEEE1149.1 Instructions and Data from the TDI/TMS inputs.
- The BYPASS register. The BYPASS register is mandatory by the standard and is used to allow TDI to propagate to TDO.
- The Instruction Register, holds the latched instruction.
- The Boundary Scan Registers (BSR), is a an array of cells of various types that are attached to the ports of the core logic and pads of the chip. The cell types include different cell types for input, output, delay sensitive input, output with enable signal and three state pads.

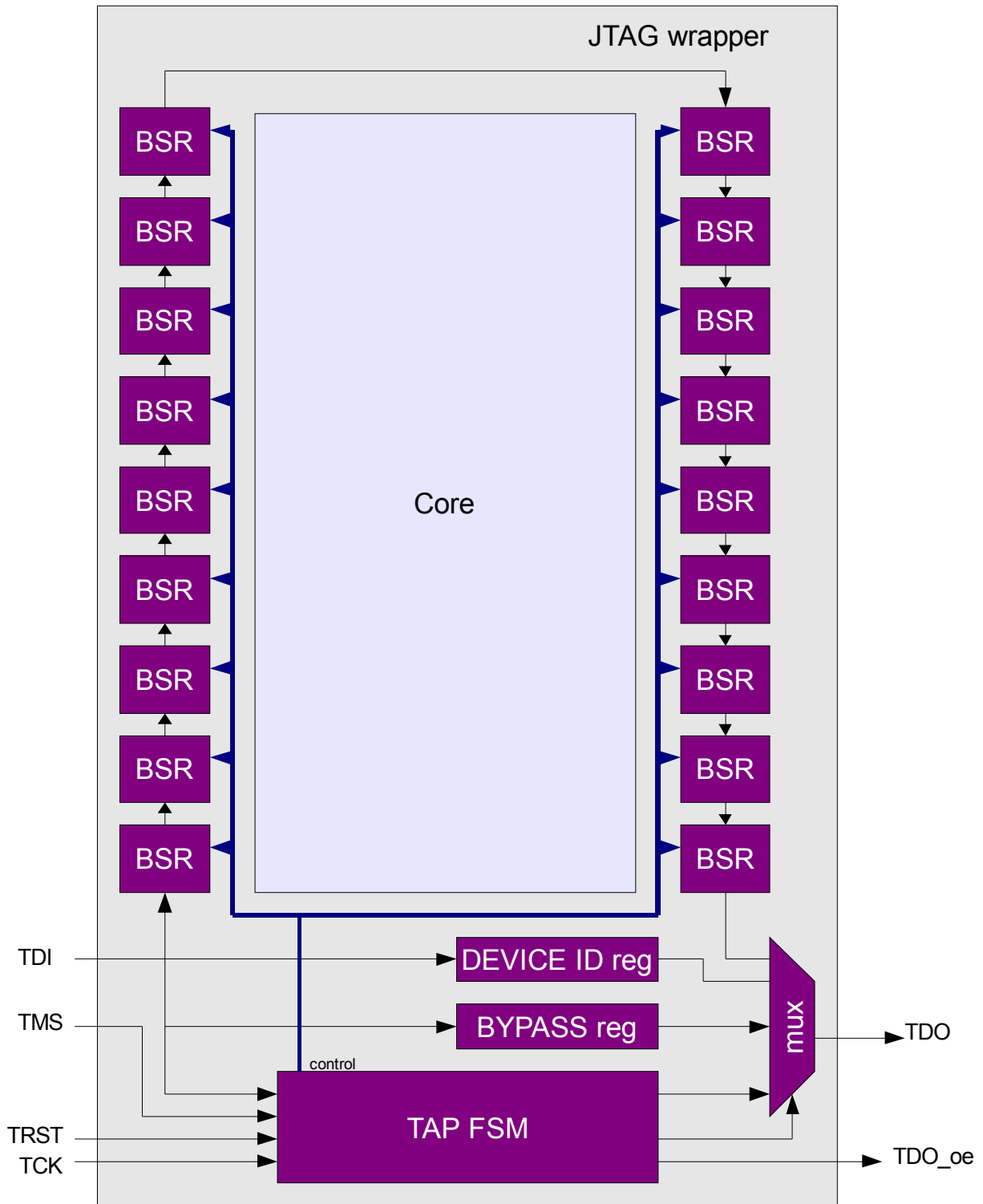


Figure 1: Block Diagram of the

### 3.2 Port Diagram

Figure 3-2 shows the ports of *JTAG wrapper*. In Figure 3-2, JTAG wrapper signals on the left side correspond to the standard JTAG 1149.1 interface while the signals on the right side are used for Boundary Scan port connections.

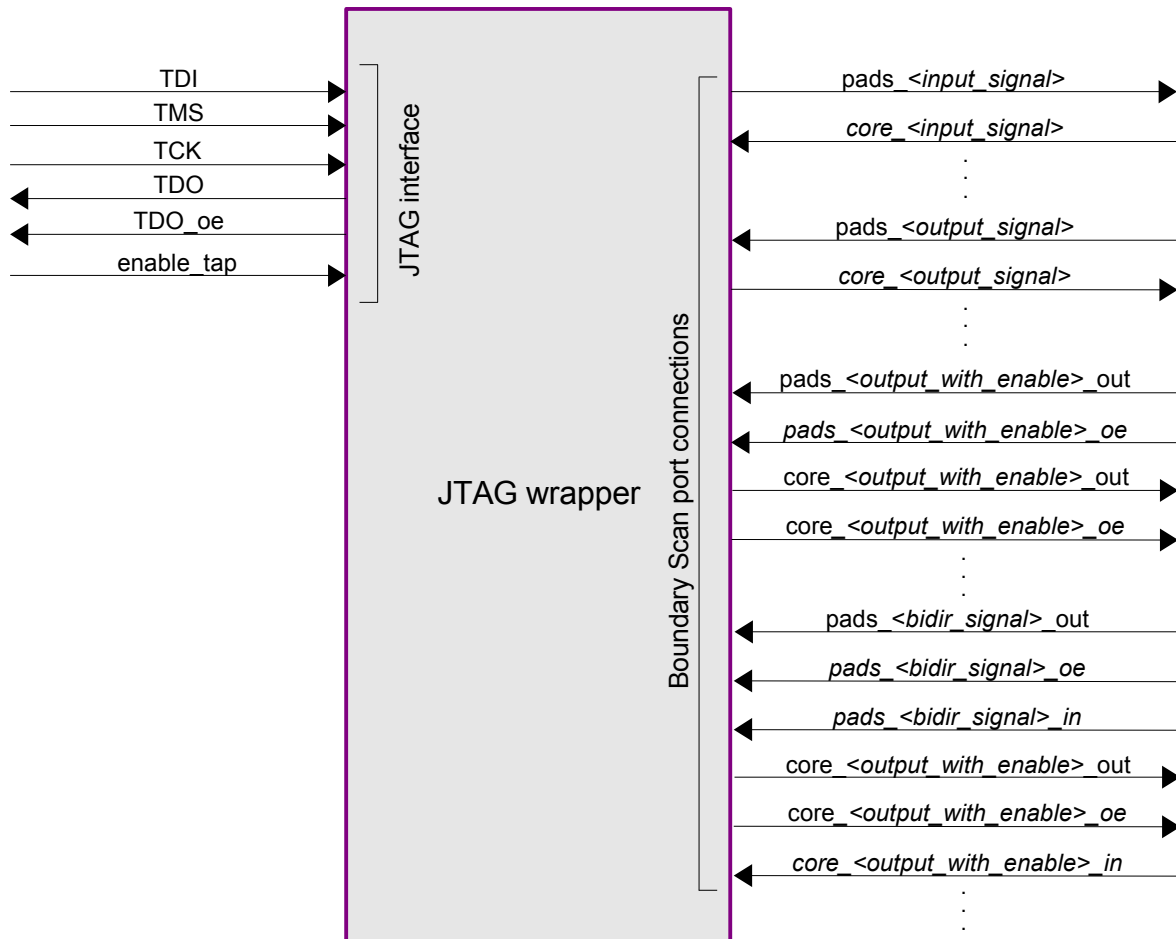


Figure 3-2 JTAG wrapper Port Diagram

### 3.3 Port Interface

Port Interface signals of JTAG wrapper are listed in Table 4-1. The boundary scan chain can be configured according to user requirements. The number, type and order of boundary scan chain registers is configurable.

Table 4-1 Product name Port list

PORT	TYPE	DESCRIPTION
TDI	Input	JTAG Test Data In
TMS	Input	JTAG Test Mode Select
TCK	Input	JTAG Test Clock
TRST	Input	JTAG Test Reset (Optional)
TDO	Output	JTAG Test Data Output
TDO_oe	Output	JTAG Test Data Output (output enable). This must be

PORT	TYPE	DESCRIPTION
		connected to a pad with output enable
enable_tap	input	Can be used as an enable signal for the TAP FSM. Otherwise should be tied to logic high (TAP is always enabled).
<b>Boundary Scan port connections (configurable)</b>		
<b>Input Signals</b>		
pads_<input signal>	Input	Data in from Pads to BSR
core_<input signal>	Output	Data out from BSR to core
<b>Output Signals</b>		
pads_<output signal>	Output	Data output from BSR to pads
core_<output signal>	Input	Data input from core to BSR
<b>Output with enable</b>		
pads_<output with enable>_out	Output	Data from BSR to pads
pads_<output with enable>_oe	Output	Data enable from BSR to pads
core_<output with enable>_out	Input	Data from core to BSR
core_<output with enable>_oe	Input	Data enable from core to BSR
<b>Bidirectional Signals</b>		
pads_<bidir signal>_out	Output	Data from BSR to pads
pads_<bidir signal>_oe	Output	Data enable from BSR to pads
pads_<bidir signal>_in	Input	Data from pads to BSR
core_<output with enable>_out	Input	Data from core to BSR
core_<output with enable>_oe	Input	Data enable from core to BSR
core_<output with enable>_in	Output	Data from BSR to core

## 4 Generator Usage

The JTAG generator employs a graphical web user interface (GUI) for configuring and generating the TAP controller and Boundary scan register components. In order to use the GUI you must sign-in on Think Silicon Ltd web site. If already registered, click on *Sign-in* link in the upper, right side of the web page. Otherwise click on *Register* link first and follow the instructions. The initial GUI page is shown in Figure 4-1.

JTAG IEEE 1149.1 TAP Controller and pad control logic

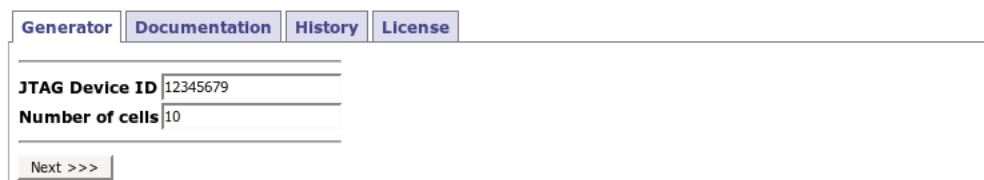


Figure 4-1 Product GUI page 1

On the next configuration page (see Figure 4-2) the user can select the exact registers to be used in the boundary scan register.

**JTAG IEEE 1149.1 TAP Controller and pad control logic**

Cell	Name	Value	Cell Type
Cell 0	clock		Input (BC4)
Cell 1	reset		Input (BC4)
Cell 2	databus0		Bidir (3 BC1)
Cell 3	databus1		Bidir (3 BC1)
Cell 4	databus2		Bidir (3 BC1)
Cell 5	databus3		Bidir (3 BC1)
Cell 6	mode		Input (BC1)
Cell 7	cs		Output with enable (2 BC1)
Cell 8	Result		Output (BC2)
Cell 9	gpio		Bidir (3 BC1)

Generate

Figure 4-2: Boundary Scan Register cell type selection

Once, all the parameters are configured, the user can click on the generate button to receive the configured circuitry.

## 5 Implementation Notes

Please follow the following guidelines for system integration.

1. System reset should internally assert the TRST signal too. This is important for setting the boundary scan control signal to default values to allow mission mode operation.
2. TRST signal is optional, but you should still connected it internally to system reset.
3. TDI, TMS and TRST signals should be connected to pads with pullup resistors to assert a logic one when floating.
4. TDO\_oe is generated using active high polarity. You may want to invert that depending on your output pads.
5. Instruction register is fixed to 4-bits:

EXTEST	0000
SAMPLE_PRELOAD	0001
IDCODE	0010
BYPASS	1111

6. Vendor IDCODE is user definable. Please note that the lsb bit must be set to 1

## 6 Deliverables

JTAG 1149.1 Generator deliverables package consists of the present document and source code files in Verilog™<sup>1</sup> HDL language. Deliverables are listed in Table 5-1.

Table 5-1 JTAG 1149.1 Generator Deliverables

File	Description
rtl/TSi_JTAG_wrapper.v	Top Level Wrapper module. Includes TAP FSM and Boundary Scan Register built according to user requirements.
rtl/tap/TSi_tap.v	JTAG TAP Controller
rtl/tap/jtag_id.v	IDCODE Register
rtl/tap/jtag_ir.v	INSTRUCTION Register
rtl/tap/TSi_jtag_fsm.v	Control FSM
rtl/tap/TSi_jtag_defines.v	Source code definitions
rtl/cells/bc_1.v	BC_1 BSR
rtl/cells/bc_2.v	BC_2 BSR
rtl/cells/bc_4.v	BC_4 (speed sensitive input)
rtl/cells/bc_oe.v	Boundary Cell , Output with enable (formed using two BC_1 cells)
rtl/cells/bc_bidir.v	Boundary Cell, Bidirectional (formed using three BC_1 cells)
doc/TSi_jtag_wrap.pdf	Documentation

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