



VLSI Design & Consultancy

DATASHEET

Async FIFO
Version 1.0

1 Overview

The Think-Silicon *Async FIFO* is a synthesizable Twin Port Memory based FIFO generator. Read and Write ports use a different clock, thus the FIFO can be used in clock domain matching applications. Use of Gray binary encoding ensures there are no transitional problems.

2 Features

- Easy to use Graphical Web User Interface
- Separate Read and Write port interfaces
- Configurable memory size
- Clock synchronization
- Gray encoding

3 Architecture

3.1 Block Diagram

Figure 3-1 represents the basic functional block of the *async_FIFO* module generated by the Silicon *Async FIFO* toolkit. The *Memory* block may be a synthesizable RTL memory module or a hard or soft memory macro. A proprietary or 3rd party memory module can be easily integrated as *Memory* block. *Ctrl & Sync* block performs clock domain synchronization and memory level control. The Gray encoding/decoding functionality is performed by the *Gray codec* functional block.

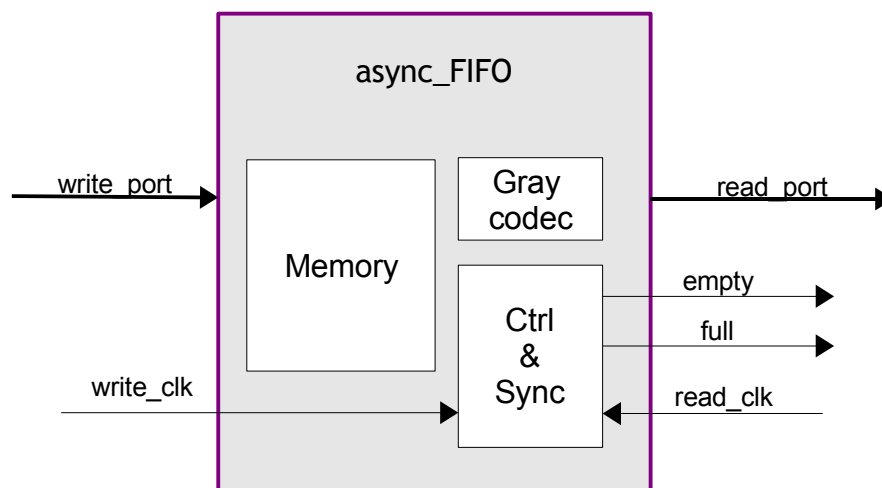


Figure 3-1 *async_FIFO* Block Diagram

3.2 Port Diagram

The *async_FIFO* Port Diagram is shown in Figure 3-2.

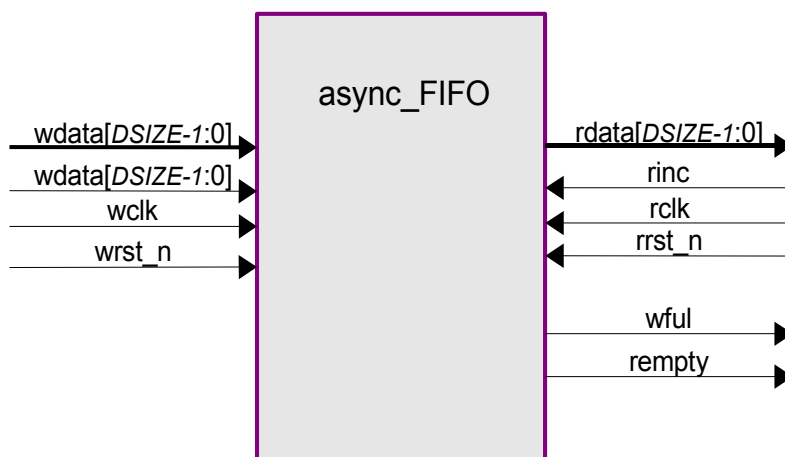


Figure 3-2 *async_FIFO* Port Diagram

3.3 Port Interface

The port signals of *async_FIFO* module are listed in Table 3-1.

Table 3-1 *async_FIFO* Port Interface

PORT	TYPE	DESCRIPTION
rdata[DSIZE-1:0]	Output	Read data Port
wfull	Output	FIFO full flag
rempty	Output	FIFO empty flag
wdata[DSIZE-1:0]	Input	Write data Port
winc	Input	Write Increment
wclk	Input	Write Clock
wrst_n	Input	Write Reset
rinc	Input	Read increment
rclk	Input	Read clock
rrst_n	Input	Read Reset

Note: The symbol DSIZE refers to the size of Read and Write data ports. It can be defined by the user through the "With" parameter in the Async FIFO GUI (see 4. Generator Usage).

4 Generator Usage

The Async FIFO generator employs a graphical web user interface (GUI) for configuring and generating the *async_FIFO* module. In order to use the GUI you must sign-in Think Silicon Ltd web site. If already registered, click on *Sign-in* link in the upper, right side of the web page. Otherwise click on *Register* link first and follow the instructions. The Async FIFO generator GUI page is shown in Figure 4-1.

As shown in Figure 4-1, the size of the *async_FIFO* can be arbitrarily defined by the user. After having completed the configuration parameters, press the *Generate* button in order to generate the *async_FIFO* module.

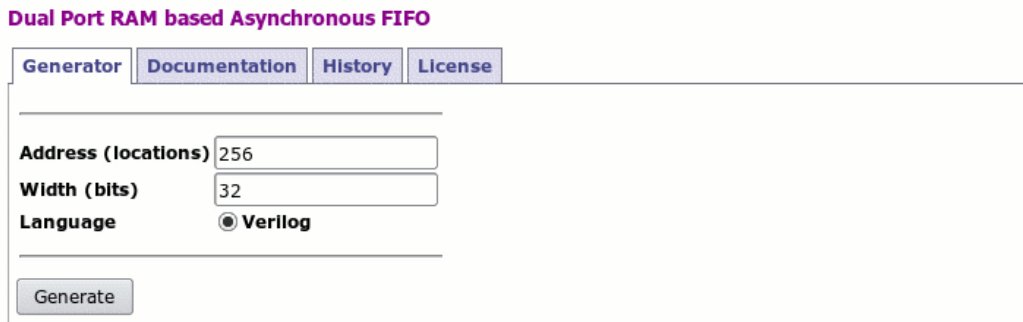


Figure 4-1. Async FIFO generator GUI

5 Deliverables

The package generated with *Async FIFO* consists of the present document and source code files in Verilog™¹ HDL language. The files are listed in Table 5-1.

Table 5-1 *async_FIFO* Deliverables

FILE	DESCRIPTION
AF_DIMENSION_fifo_gray_dc.v	<i>async_FIFO</i> top module
AF_DIMENSION_async_cmp.v	<i>async_FIFO</i> level
AF_DIMENSION_fifomem.v	Memory block wrapper
AF_DIMENSION_rptr_empty.v	Read port empty monitor
AF_DIMENSION_wptr_full.v	Write port full monitor
AF_DIMENSION_parameters.txt	<i>async_FIFO</i> generation parameters
TSi_asyncFIFO.pdf	The present document

Note: “AF” stands for Asynchronous FIFO. The “DIMENSION” substring refers to memory dimensions and has the form “memory locations x location size in bits”, “256x32” for example.

¹ Verilog is a trademark of Cadence Design Automation. (<http://www.cadence.com>)

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