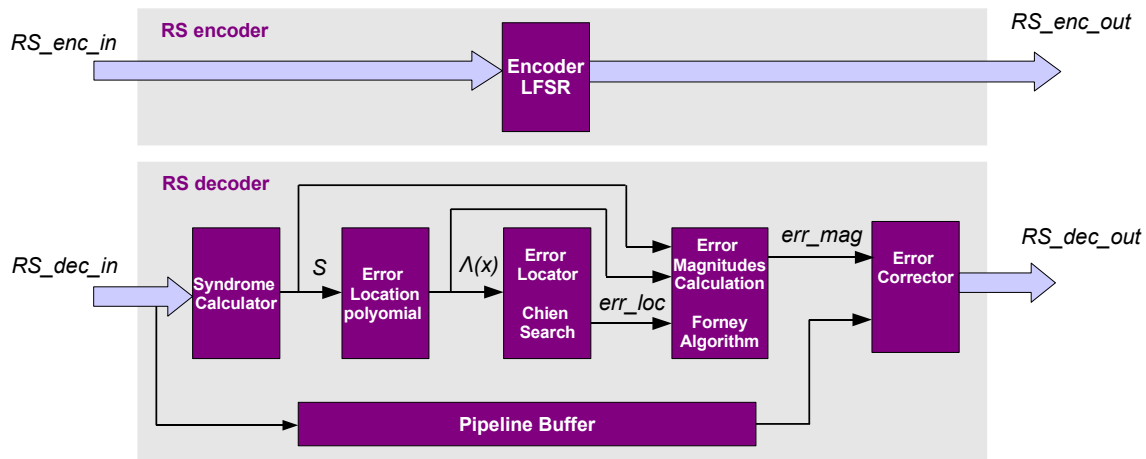


## Reed Solomon RS(n,k) Encoder/Decoder

parameterizable IP core



### Standard Features

- Reed Solomon RS(n,k) encoder/decoder
  - $n$  : RS(n,k) block length in symbols
  - $k$  : number of RS(n,k) block data symbols
  - $n - k$  : number of RS(n,k) block parity symbols
  - $t$  : RS(n,k) code error capability ( $2t = n - k$ )
  - $m$  : symbol size in bits, ( $m = \log n$ ) corresponds to GF(2<sup>m</sup>) Galois Field
- Fully parameterizable Verilog RTL code for any valid  $n, k$  set
- Serial  $m$ -bit symbol feed
- Serial  $m$ -bit symbol output
- Error-detection capability up to  $2t$  errors
- Error-correction capability up to  $t$  errors
- Efficient GF(2<sup>m</sup>) multiplier scheme
- Fully-synthesizable Verilog HDL code
- Single-clock domain

### Optional-Custom Features & Services

- Programmable RS(n,k) code operation
  - The IP core can support various RS(n,k) codes
  - $n, k$  parameters are programmed through registers
- Custom Implementations
  - Architectural (Parallel, Serial, Pipeline, feed-through)
  - Algorithmic (Peterson-Gorestein-Zier, Euclidean, etc)
  - RS generator polynomial (custom or from predefined lists)
  - Galois Field GF(2<sup>m</sup>) definition (custom or from predefined lists)
- Optimized version (area, speed, throughput) for specific  $n, k$  or range of  $n, k$
- Extra error-correction capabilities
- Custom Verification models & Testbenches
  - Verilog
  - Matlab
- Synthesis scripts & Netlist
  - FPGA
  - ASIC