



Computer Graphics Solutions

DATASHEET

DMAC
Version 1.02

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Questions or comments may be directed to:

Think Silicon Ltd
Suite B12
Patras Science Park
Rion Achaïas 26504
Greece

web: <http://www.think-silicon.com>
email: info@think-silicon.com
Tel: +30 2610 911543
Fax: +30 2610 911544

Document Revision History

Editor	Revision	Date	DESCRIPTION
GS	1.00	28/02/2008	Initial Version
MM	1.01	26/08/2008	Extra figures for channel configurations and register descriptions added
GS,TR	1.02	25/07/2011	Register set review, document format

1 Overview

The Think-Silicon DMAC is a web configurable generator for DMA Controller.

2 Features

- AMBA AHB 2.0 compliant
- Configurable DMA transfers
 - AHB to AHB
 - AHB to FIFO
 - FIFO to AHB
- Configurable number of channels
- Configurable FIFO size
- AMBA AHB Slave Interface for register programming
- AMBA AHB Master Interface(s) for DMA transfers
- FIFO access Interface(optional) for DMA transfers
- One FIFO per channel
- Different Clock Domains at FIFO Interface and AMBA AHB Bus Interface
- AMBA AHB Master supports burst transfers
- Byte alignment supported
- Direct Access to FIFO data
- Programmable Interrupt lines

3 Architecture

3.1 Block Diagram

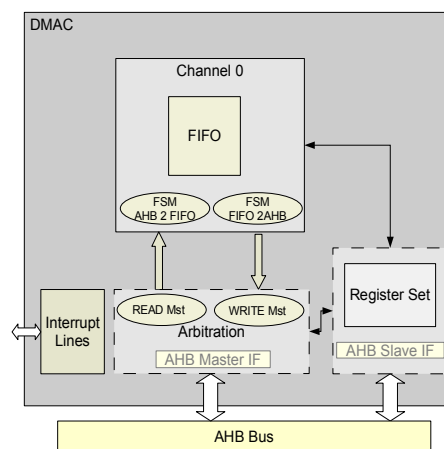


Figure 3-1 Single Channel AHB to AHB DMA transfers (common AHB Bus)

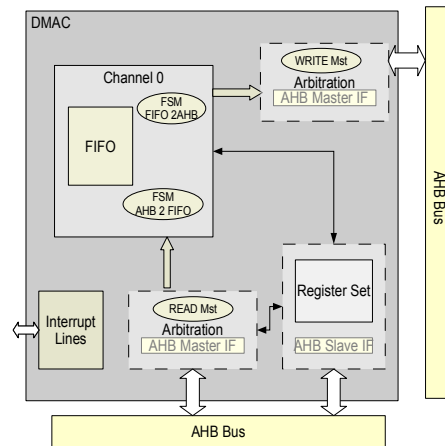


Figure 3-2 Single Channel AHB to AHB DMA transfers (separate AHB Buses)

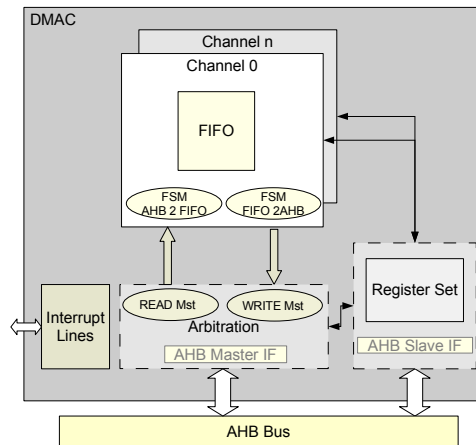


Figure 3-3 Multiple Channel AHB to AHB DMA transfers (common AHB Bus)

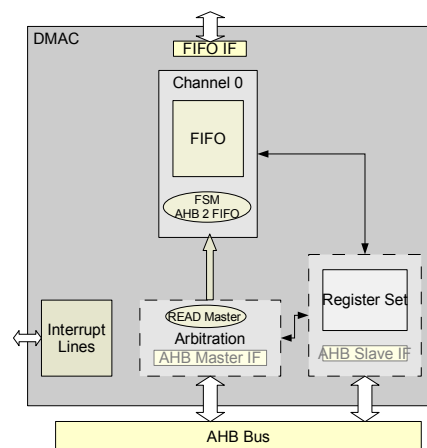


Figure 3-4 Single Channel AHB to FIFO DMA transfers

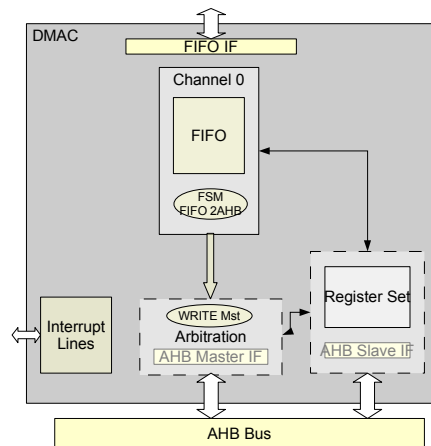


Figure 3-5 Single Channel FIFO to AHB DMA transfers

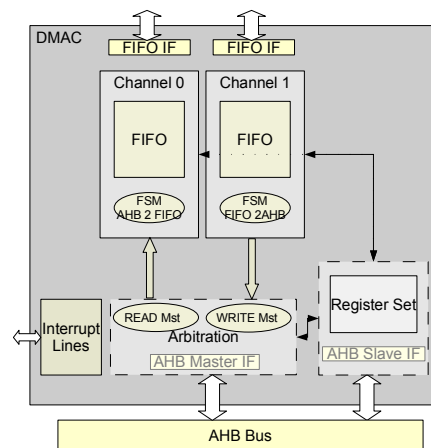


Figure 3-6 Multiple Channel AHB to FIFO, FIFO to AHB DMA transfers

3.2 Port Interface

Table 3-1 AHB Master Port list (Optional: second IF in case of different AHB Buses : Figure 3-2)

PORT	TYPE	DESCRIPTION
HCLK	Input	Bus Clock
HRESETn	Input	Bus Reset
HLOCK_mst	Output	Bus Lock
HBUSREQ_mst	Output	Bus Request
HGRANT_mst	Input	Bus Grant
HADDR_mst[31:0]	Output	Address Bus
HTRANS_mst[1:0]	Output	Transfer Type

PORT	TYPE	DESCRIPTION
HBURST_mst[2:0]	Output	Burst Type
HSIZE_mst[2:0]	Output	Transfer Size
HWRITE_mst	Output	Transfer Direction
HPROT_mst[3:0]	Output	Protection Control
HWDATA_mst[31:0]	Output	Write Data Bus
HRDATA_mst[31:0]	Input	Read Data Bus
HREADY_mst	Input	Transfer Done
HRESP_mst[[1:0]	Input	Transfer Response

Table 3-2 AHB Slave Port list

PORT	TYPE	DESCRIPTION
HTRANS_slv	Input	Transfer Type
HSEL_slv	Input	Peripheral selection signal
HSIZE_slv	Input	Transfer Size
HADDR_slv[31:0]	Output	Address Bus
HWDATA_slv[31:0]	Input	Write Data Bus
HRDATA_slv[31:0]	Output	Read Data Bus
HRESP_slv[[1:0]	Output	Transfer Response
HREADY_slv	Output	Transfer Done

Table 3-3 FIFO Interface Port list (Optional: One for every Channel that with FIFO IF)

PORT	TYPE	DESCRIPTION
Read_active	Input	Read Request
Read_size[1:0]	Input	Size (in bytes) of active read
Read_clk	Input	Read Clock
Ready_to_read	Output	FIFO is ready to read
Read_data[31:0]	Output	Data read from FIFO
Write_active	Input	Write Request
Write_size[1:0]	Input	Size (in bytes) of active write
Write_clk	Input	Write Clock
Ready_to_write	Output	FIFO is ready to be Written
Write_data[31:0]	Input	Write data to FIFO

Table 3-4 Miscellaneous ports

PORT	TYPE	DESCRIPTION
Irq	Output	Interrupt request
Endianness	Input	Endianness control: 0 Little Endiannes, 1: Big Endianness

4 Register Set

The following tables describe register set per channel for various DMAC configurations

Table 5-1 Register Set (Bus to Memory)

ADDRESS OFFSET	REGISTER		DESCRIPTION
0x00	Control	R/W	Bits 31..9: reserved Bit 8: Zero Latency:when set, FIFO read port operates without latency Bit 7: reserved Bit 6: discard fifo reset Bit 5: read fifo reset Bit 4: write fifo reset Bit 3: dma start Bit 2: fifo read empty flag Bit 1: fifo write full flag Bit 0: dma lock
0x04	fifo_wpointer	R/O	contains the value of actual FIFO Write pointer
0x08	source_address	R/W	DMA Source Address
0x0c	dma_length	R/W	Length of DMA in bytes
0x10	ahb_conf_reg	R/W	Bits 31..1: reserved Bit 0: Locked AHB Transfers
0x14	fifo_wspace	R/O	Number of Flushed/Discarded fifo bytes
0x18	reserved	R/O	
0x10	full_thresh	R/W	Full Threshold:If bytes stored in FIFO are more than <i>full_thresh</i> , interrupt generation will occur
0x20	empty_thresh	R/W	Empty threshold, if bytes stored in FIFO are less than <i>empty_thresh</i> , interrupt generation will occur
0x24	fifo_rdata	RO	FIFO direct Data Read register

Table 5-2 Register Set (Memory to Bus)

ADDRESS OFFSET	REGISTER		DESCRIPTION
0x00	Control_register	R/W	Bits 31..9: reserved Bit 8: Zero Latency: when set, FIFO read port operates without latency Bit 7: Flush fifo data: set dma length to current fifo size, dma will end when all data are transferred over AHB Bus Bit 6: discard fifo data Bit 5: read fifo reset Bit 4: write fifo read empty flag Bit 1: fifo write full flag Bit 0: dma lock
0x04	fifo_rpointer	RO	FIFO Read pointer
0x08	dest_address	R/W	DMA Destination Address
0x0c	dma_length	R/W	Length of DMA in bytes
0x10	ahb_cont_reg	R/W	Bits 31..1: registered Bit 0: Locked AHB Transfers
0x14	num_of_flushed_bytes	RO	Number of Flushed/Discarded fifo bytes
0x18	reserved		
0x10	full_thresh	R/W	Full threshold: If bytes stored in FIFO are more than <i>full_thresh</i> , interrupt generation will occur
0x20	empty_thresh	R/W	Empty threshold, if bytes stored in FIFO are less, than <i>empty_thresh</i> interrupt will occur
0x24	direct_fifo_read_data	RO	FIFO direct Data Read register

Table 5-2 Register Set (Bus2Bus)

ADDRESS OFFSET	REGISTER		DESCRIPTION
0x00	Control_register	R/W	Bits 31..9: reserved Bit 8: Zero Latency: when set, FIFO read port operates without latency Bit 7: reserved Bit 6: discard fifo data Bit 5: read fifo reset Bit 4: write fifo reset Bit 3: dma start Bit 2: fifo read empty flag Bit 1: fifo write full flag Bit 0: dma lock
0x04	source_address	R/W	DMA Source Address
0x08	dest_address		DMA Destination Address
0x0c	dma_length	R/W	Length of DMA in bytes
0x10	fifo_wpointer	RO	FIFO Write pointer
0x14	fifo_rpointer	RO	FIFO Read pointer
0x18	ahb_conf_reg	R/W	Bits 31..1: Reserved Bit 0: Locked AHB Transfers

0x10	full_thresh	R/W	Full Threshold: If bytes stored in FIFO are more than <i>full_thresh</i> , interrupt generation will occur
0x20	empty_thresh	R/W	Empty threshold, If bytes stored in FIFO are less than <i>empty_thresh</i> , interrupt generation will occur

5 Generator Usage

The DMAC generator employs a graphical web user interface (GUI) for configuring and generating the DMA Controller. In order to use the GUI you must sign-in Think Silicon Ltd web site. If already registered, click on *Sign-in* link in the upper, right side of the web page. Otherwise click on *Register* link first and follow the instructions. The initial GUI page is shown in Figure 4-1.

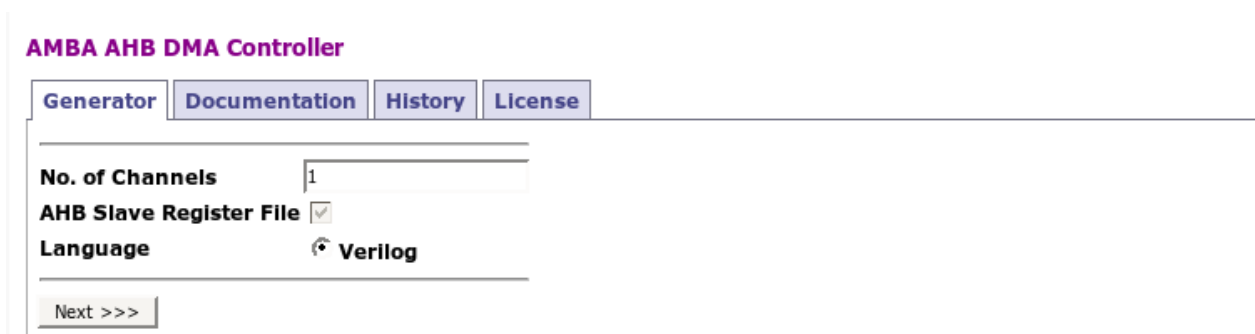


Figure 4-1 AMBA AHB DMA Engine GUI page 1

As depicted in Figure 4-1, the number of supported DMA Channels is configurable. Click *Next* and the second page of DMAC(Figure 4-2.) appears.

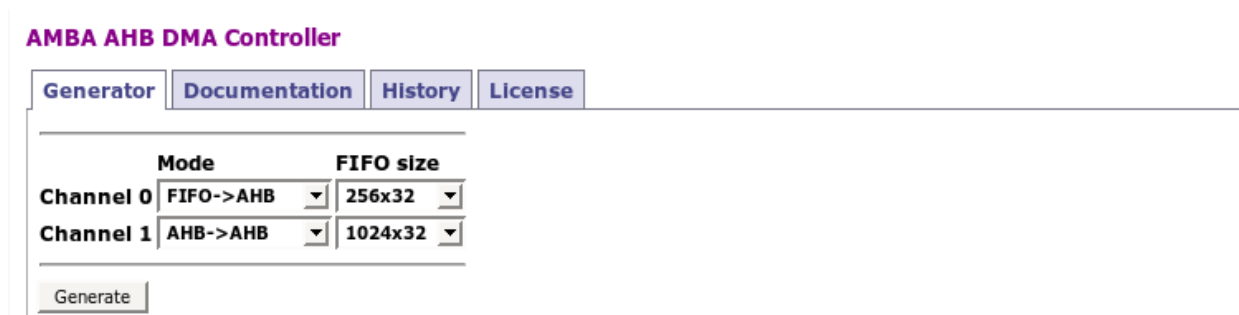


Figure 4-2 AMBA AHB DMA Engine GUI page 2

As shown in Figure 4-2, each channel mode can be selected from following:

- AHB to FIFO : Data transfers from AHB Bus to FIFO, FIFO IF for Data Read
- FIFO to AHB : Data transfers from FIFO to AHB Bus, FIFO IF for Data Write
- AHB to AHB : Data transfers from AHB Bus to AHB Bus
- AHB to different AHB : Data transfers from AHB Bus to different AHB Bus

FIFO size can be selected from the following sizes:

- 128x32, 256x32, 512x32, 1024x32, 2048x32

After having completed the the fields depicted in Figure 4-2, click on the *Generate* button. The generated DMAC package will be sent to the email address given in the registration step.