

**Think** Silicon

VLSI Design & Consultancy

**DATASHEET**

**BusBuilder for AMBA<sup>®</sup> APB<sup>™</sup>**  
**Version 1.0**



## 1 Overview

The Think-Silicon *BusBuilder for AMBA® APB™*<sup>1</sup> is a web configurable AMBA AHB™ to AMB APB™ bus Bridge generator.

## 2 Features

- Easy to use Graphical Web User Interface
- Configurable number of AMBA APB slave devices
- Configurable AMBA APB port names prefixes and suffixes
- Configurable AMBA AHB and AMBA APB address and data bus size
- Flexible AMBA APB address bus decoding scheme for AMBA APB slave devices

## 3 Architecture

### 3.1 Block Diagram

Figure 3-1 represents the basic functional block of the *Bridge for AMBA AHB2APB conversion* system generated by the Silicon *BusBuilder for AMBA™ APB* toolkit.

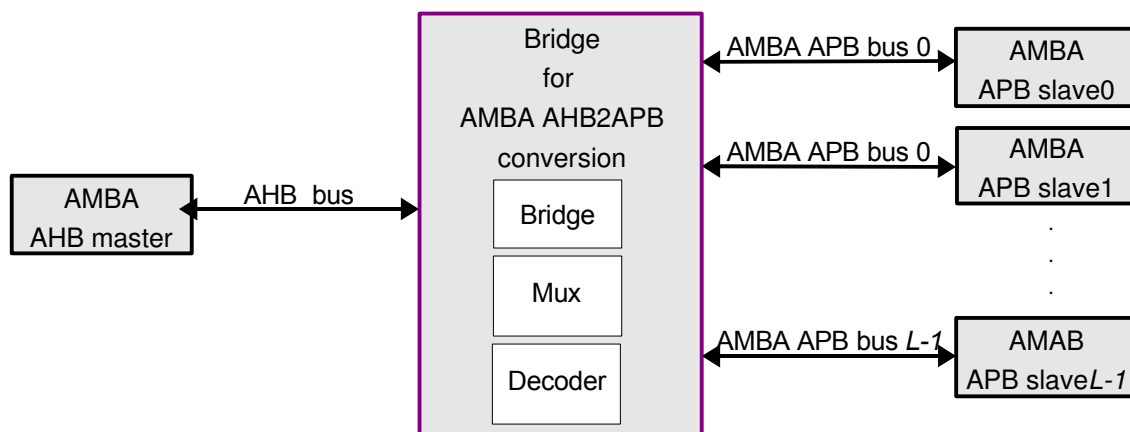


Figure 3-1. *Bridge for AMBA AHB2APB conversion* system Block Diagram

As shown in Figure 3-1 *Bridge for AMBA AHB2APB conversion* system provides one port for the external AMBA AHB master and  $L-1$  ports for external AMBA APB slaves. The number of supported slaves is configurable. The *Bridge for AMBA AHB2APB conversion* system blocks perform AHB2APB bus conversion, AMBA APB bus decoding and AMBA APB Bus multiplexing functions.

The *Bridge for AMBA AHB2APB conversion* system is able to route traffic from the AMBA AHB master device

<sup>1</sup> AMBA is a trademark of ARM Limited. Cambridge, UK (<http://www.arm.com>)

to any of the  $L$  AMBA APB slave devices and vice-versa. Figure 3-2 shows an AMBA AHB master device and  $L$  AMBA APB slave devices connected to the *Bridge for AMBA AHB2APB conversion* system. All possible routing paths are also depicted.

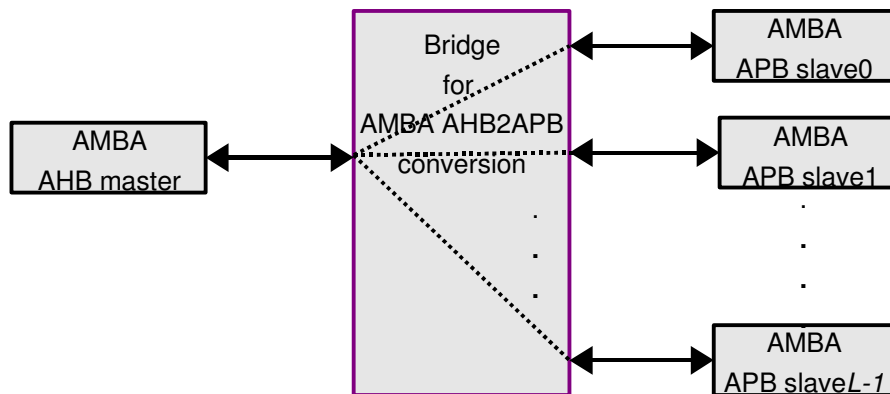


Figure 3-2. *Bridge for AMBA AHB2APB conversion* system routing functionality

### 3.2 Port Diagram

Figure 3-3 shows the *Bridge for AMBA AHB2APB conversion* ports. Port descriptions are defined in the following sections. The symbol  $j$  refers to one of the  $L$  external AMBA APB slave devices connected to the AHB2PABBus system ( $j=0,1,2, \dots, L-1$ ). AMBA AHB and APB address bus size is defined by the *ADDRSIZE* parameter, hence the convention  $HADDR[ADDRSIZE-1:0]$ ,  $PADDR[ADDRSIZE-1:0]$ , etc. is used. Similarly AMBA AHB and AMBA APB data bus size is defined by the *DATASIZE* parameter, hence the convention  $HWDATA[HDATASIZE-1:0]$ ,  $HRDATA[HDATASIZE-1:0]$  etc. is used.

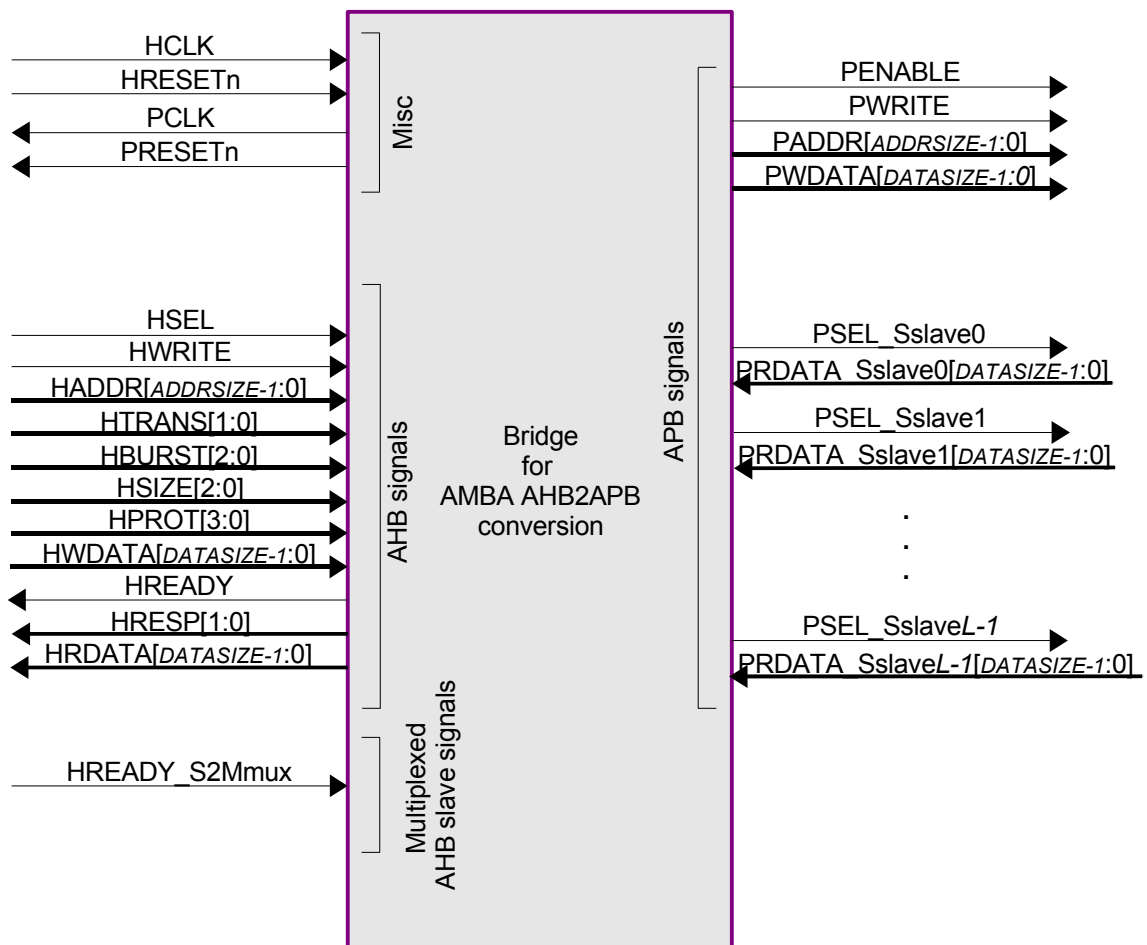


Figure 3-3 Bridge for AMBA AHB2APB conversion Port Diagram

### 3.3 Port Interface

Bridge for AMBA AHB2APB conversion port signals are listed in Table 3-1.

Table 3-1 Bridge for AMBA AHB2APB conversion Port list

PORT	TYPE	DESCRIPTION
HCLK	Input	AMBA AHB HCLK
HRESETn	Input	AMBA AHB HRESETn
PCLK	Output	AMBA APB PCLK
PRESETn	Output	AMBA APB PRESETn
HSEL	Input	AMBA AHB HSEL signal from AMBA AHB master device
HWRITE	Input	AMBA AHB HWRITE signal from from AMBA AHB master device
HADDR[ADDRSIZE-1:0]	Input	AMBA AHB HADDR bus from AMBA AHB master device
HTRANS[1:0]	Input	AMBA AHB HTRANS control signals from AMBA AHB master device

PORT	TYPE	DESCRIPTION
HBURST[2:0]	Input	AMBA AHB HBURST control signals from AMBA AHB master device
HSIZE[2:0]	Input	AMBA AHB HSIZE control signals from AMBA AHB master device
HPROT[3:0]	Input	AMBA AHB HPROT control signals from AMBA AHB master device
HWDATA[ <i>DATASIZE</i> -1:0]	Input	AMBA AHB HWDATA control signals from AMBA AHB master device
HREADY	Output	AMBA AHB HREADY control signal to AMBA AHB master device
HRESP[1:0]	Output	AMBA AHB HRESP signals to AMBA AHB master device
HRDATA[ <i>DATASIZE</i> -1:0]	Output	AMBA AHB HRDATA bus to AMBA AHB master device
HREADY_S2Mmux	Input	Multiplexed AMBA AHB HREADY signal from other AMBA AHB slave devices
PENABLE	Output	AMBA APB PENABLE signal to AMBA APB slave devices
PWRITE	Output	AMBA APB PWRITE signal to AMBA APB slave devices
PADDR[ <i>ADDRSIZE</i> -1:0]	Output	AMBA APB PADDR bus to AMBA APB slave devices
PWDATA[ <i>DATASIZE</i> -1:0]	Output	AMBA APB PWDATA bus to AMBA APB slave devices
PSEL_Sslave <sub><i>j</i></sub>	Output	AMBA APB PSEL signal to AMBA APB slave device <i>j</i>
PRDATA_Sslave <sub><i>j</i></sub> [ <i>DATASIZE</i> -1:0]	Input	AMBA APB PRDATA bus from AMBA APB slave device <i>j</i>
PENABLE	Output	AMBA APB PENABLE strobe signal
PWRITE	Output	AMBA APB PWRITE signal
PADDR[ <i>HADDRSIZE</i> -1:0]	Output	AMBA APB PWRITE signal
PWDATA[ <i>HDATASIZE</i> -1:0]	Output	AMBA APB PWDATA write data bus
PSEL <sub><i>j</i></sub>	Output	AMBA APB PSEL signal to AMBA APB slave device <i>j</i>
PRDATA <sub><i>j</i></sub> [ <i>HDATASIZE</i> -1:0]	Input	AMBA APB PRDATA read data bus from AMBA APB slave device <i>j</i>

**Notes:**

1. The symbol *j* refers to one of the *L* external AMBA APB slave devices connected to the Bridge for AMBA AHB2APB conversion system (*i*=0, 1, 2, ..., *L*-1). 3

2 The *ADDRSIZE* parameter defines the size of AMBA AHB and address buses  $2 \leq HADDRSIZE \leq 16$ .

3. The *DATASIZE* parameter defines the size of AMBA AHB and AMBA APB data buses  $2 \leq DATASIZE \leq 32$ .

4. There is the option to define custom prefixes and suffixes for AMBA AHB port names. (The port names in Table 4-1 have no prefixes added).

The default suffixes are used i.e. slave0, slave1, ... slave<sub>*j*</sub> for AMBA APB slave signals.

## 4 Generator Usage

The *BusBuilder for AMBA APB* generator employs a graphical web user interface (GUI) for configuring and generating the *Bridge for AMBA AHB2APB conversion* system. In order to use the GUI you must sign-in Think Silicon Ltd web site. If already registered, click on *Sign-in* link in the upper, right side of the web page. Otherwise click on *Register* link first and follow the instructions. The initial GUI page is shown in Figure 4-1.

[Sign In](#) | [Register](#)

**AMBA AHB to APB Bridge generator**

Generator Documentation History License

bus name

Slaves

Address size

Data size

Next >>>

Figure 4-1 *BusBuilder for AMBA APB* GUI page

In GUI page 1 click the *Next* button.

As depicted in Figure 4-1, the number of supported AMBA APB slave devices , the size of AMBA AHB and AMBA APB address and data buses are configurable. It also is possible to attached a prefix to the names of the AMBA AHB and APB ports.

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Slaves : 4

Slave	Name	Decode bits	Address
Slave name 0:	<input type="text" value="slave0"/>	<input type="text" value="4"/>	<input type="text" value="0x0000"/>
Slave name 1:	<input type="text" value="slave1"/>	<input type="text" value="4"/>	<input type="text" value="0x1000"/>
Slave name 2:	<input type="text" value="slave2"/>	<input type="text" value="4"/>	<input type="text" value="0x2000"/>
Slave name 3:	<input type="text" value="slave3"/>	<input type="text" value="4"/>	<input type="text" value="0x3000"/>

Generate

Figure 4-2 *BusBuilder for AMBA APB* GUI page 2

As shown in Figure 4-2, the names of AMBA APB slave devices can be modified. These names will be added as suffixes to the AMBA APB port names.

Decoding scheme of AMBA APB slave devices is also configurable according to the following terms:

1. The number of the most significant AMBA APB address bus bits used for decoding can be defined in *Decode bits* field for every AMBA AHB slave device.
2. The value of the decoding AMBA APB address bus bits that corresponds to each one of the AMBA APB slave devices.

After having completed the the fields depicted in Figure 4-2, click on the *Generate* button. The generated *Bridge for AMBA AHB2APB conversion* package will be sent to the email address given in the registration step.

## 5 Deliverables

The package generated with *BusBuilder for AMBA APB* generator consists of the present document and source code files in Verilog™<sup>2</sup> HDL language. The files are listed in Table 5-1.

Table 5-1 *BusBuilder for AMBA APB* Deliverables

FILE	DESCRIPTION
<i>PREFIX</i> _APBsystemAPBBus.v	Bridge for AMBA AHB2APB conversion top module
<i>PREFIX</i> _APBsystemAPBCtrl.v	AMBA AHB to AMBA APB bus converter
<i>PREFIX</i> _APBsystemAHBDec.v	AMBA APB address bus decoder
<i>PREFIX</i> _APBsystemAPBMux.v	AMBA APB bus multiplexer
parameters.txt	Bridge for AMBA AHB2APB conversion system parameters
./doc/TSi_AHB2APBBus.pdf	The present document

Notes: The *PREFIX* string can be defined by the user in the field bus name of web GUI (see Figure 4-1)

<sup>2</sup> Verilog is a trademark of Cadence Design Automation. (<http://www.cadence.com>)

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