



VLSI Design & Consultancy

DATASHEET

**Register File for AMBA[®] AHB[™]
Version 1.0**

1 Overview

The Think-Silicon *Registers* for AMBA[®] ¹ AHB[™] is a web configurable register file generator supporting AMBA[®] ² AHB[™] bus interface.

2 Features

- Easy to use Graphical Web User Interface
- Configurable number of registers
- Configurable register names
- Fully configurable Read Data Path scheme
- Word (4-bytes) aligned address decoding scheme
- Optional *Read Trigger* and *Write Trigger* ports option for each register

3 Architecture

4 Block Diagram

Figure 3-1 represents the Block Diagram of the *Register File* system generated by the *Registers for AMBA AHB* toolkit.

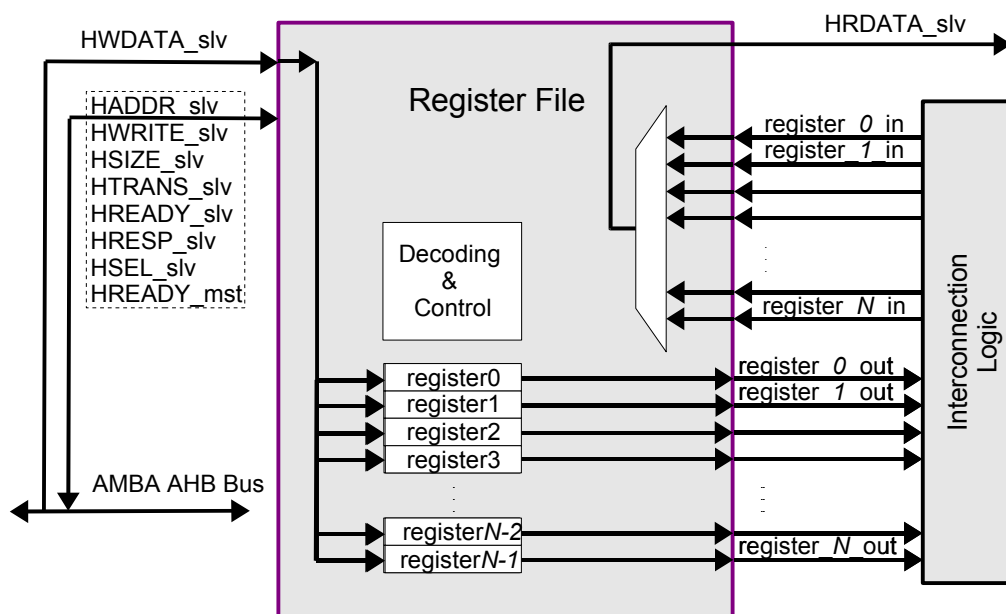


Figure 3-1. *Register File* system Block Diagram (*N* registers are supported)

Register File system provides an AMBA AHB slave interface for connecting an external AMBA AHB master device. The number of 32-bit registers is configurable. The dedicated register output ports are loaded with the contents of each register. On the other hand the dedicated register input ports are multiplexed internally and drive the HRDATA_slv AMBA AHB read data bus. Through a custom external Interconnection Logic, a fully configurable Read Data Path scheme can be built. According to that scheme any of the 32-bit register

¹ AMBA is a trademark of ARM Limited. Cambridge, UK (<http://www.arm.com>)

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contents can be assigned to any register address. For example when a register is read the 32-bit returned value could be the contents of the very same register, the contents any other register, a combination of the contents of two or more registers, a 32-bit combination of ones and zeros or a combination of all previously mentioned schemes. Further information about interconnecting *Register File* ports and integrating *Register File* into a design is given in the following paragraphs

5 Port Diagram

Figure 3-2 shows the Port Diagram of an *Register File* system supporting *N* registers.

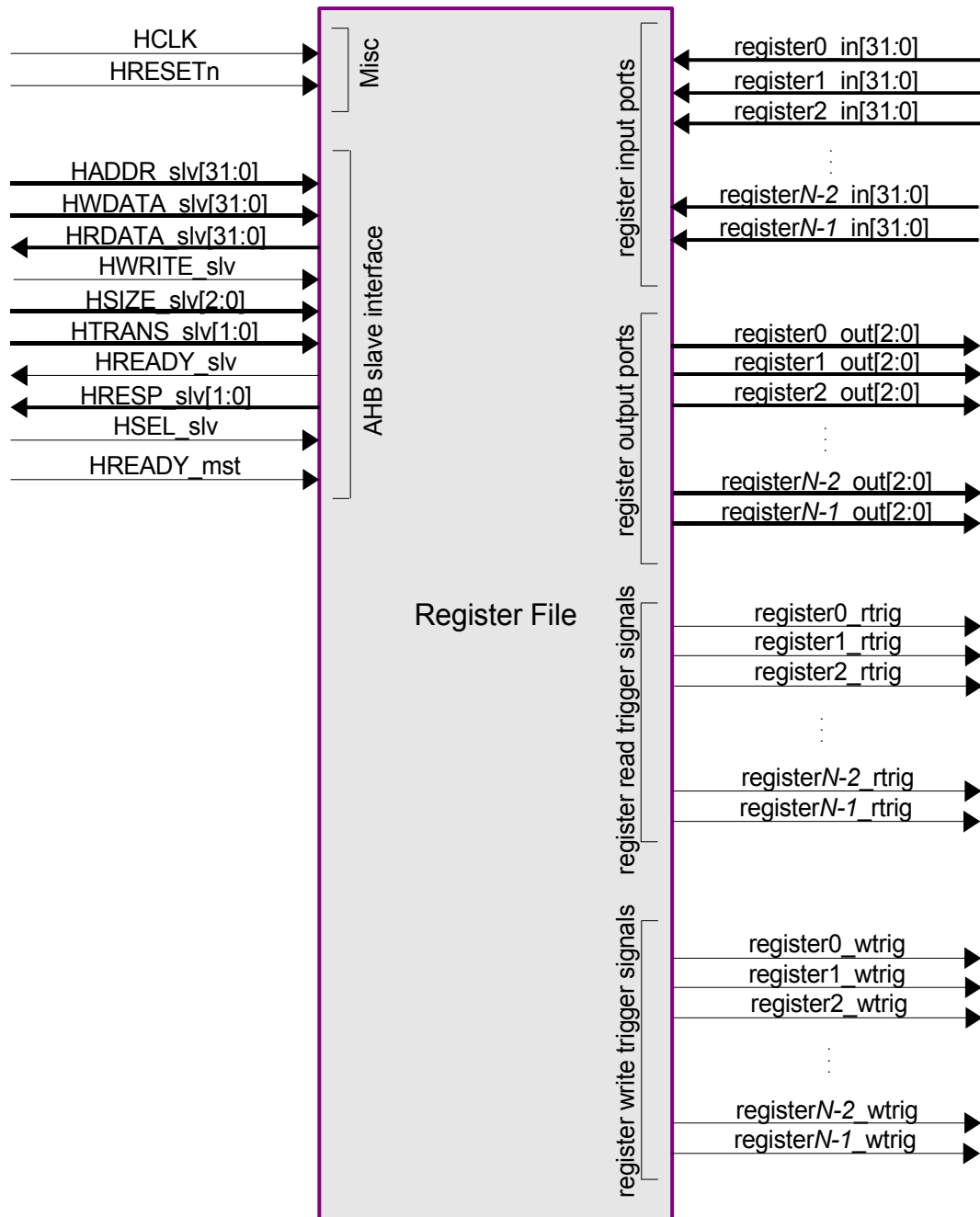


Figure 3-3 *Register File* Port Diagram

6 Port Interface

Register File port signals are listed in Table 4-1.

Table 4-1 Register File Port list

PORT	TYPE	DESCRIPTION
HCLK	Input	AMBA AHB HCLK
HRESETn	Input	AMBA AHB HRESETn
HADDR_slv[31:0]	Input	AMBA AHB HADDR address bus
HWDATA_slv[31:0]	Input	AMBA AHB HWADA write data bus
HRDATA_slv[31:0]	Output	AMBA AHB HRADA read data bus
HWRITE_slv	Input	AMBA AHB HWRITE signal
HSIZE_slv[2:0]	Input	AMBA AHB HSIZE signals
HTRANS_slv[1:0]	Input	AMBA AHB HTRANS signals
HREADY_slv	Output	AMBA AHB HREADY signal to external AMBA AHB master device
HRESP_slv[1:0]	Output	AMBA AHB HRESP signals
HSEL_slv	Input	AMBA AHB HSEL signal
HREADY_mst	Input	AMBA AHB HREADY signal (multiplexed AMBA AHB HREADY output signals from all AMBA AHB slave devices of the external AMBA AHB bus system)
register _i _in[31:0]	Output	Register <i>i</i> input port
register _i _out[31:0]	Output	Register <i>i</i> input port
register _i _wtrig	Output	Write trigger signal for register <i>i</i>
register _i _rtrig	Input	Read trigger signal for register <i>i</i>

Note: The symbol *i* refers to one of the *N* internal registers of the Registers for AMBA AHB system (*i*=0,1,2, ..., *N*-1).

7 Generator Usage

The Registers for AMBA AHB generator employs a graphical web user interface (GUI) for configuring and generating the Register File system. In order to use the GUI you must sign-in Think Silicon Ltd web site. If already registered, click on Sign-in link in the upper, right side of the web page. Otherwise click on Register link first and follow the instructions. The initial GUI page is shown in Figure 4-1.

[Sign in](#) | [Register](#)

Configurable AHB Register generation

The screenshot shows a web interface for generating AMBA AHB registers. At the top, there are four tabs: 'Generator' (selected), 'Documentation', 'History', and 'License'. Below the tabs, there are two input fields: 'Register File name' with the value 'AHBreg' and 'Number of Registers' with the value '16'. At the bottom of the form, there is a button labeled 'Next >>>'.

Figure 4-1 Registers for AMBA AHB generator GUI page 1

As shown in Figure 4-1, the number of the registers and the register file name can be defined by the user.

Click *Next* and the second page of *Registers for AMBA AHB* generator GUI (Figure 4-2.) appears.

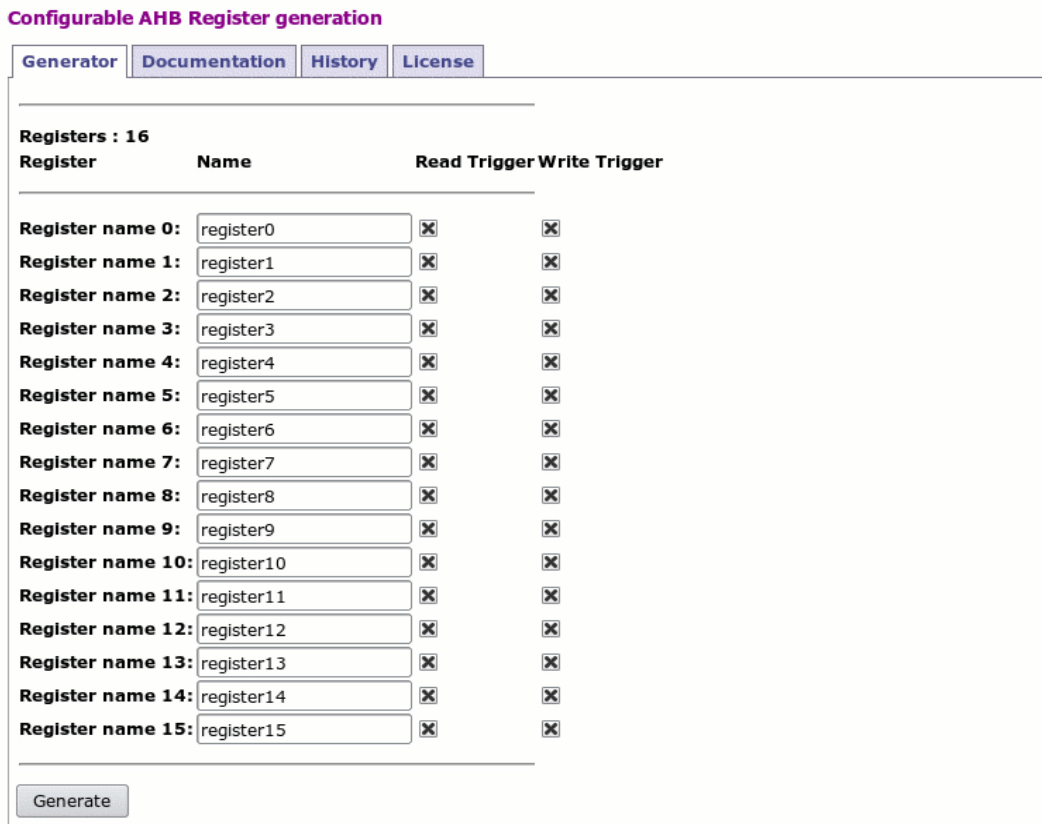


Figure 4-2 *Registers for AMBA AHB* generator GUI page 2

As shown in Figure 4-2, the names of registers can be arbitrarily defined by the user. There is also the option to implement indicator signals for successful read and write register access, simply by ticking the *Read Trigger* and *Write Trigger* boxes.

8 Interfacing Register File

Register File system provides dedicated register output and input ports. Each one of the N $register_i_out[31:0]$ output ports ($i=0,1,2,\dots,N-2,N-1$, $N \equiv$ number of registers) continuously reflects the value of the corresponding register contents.

All $register_i_in[31:0]$ input ports are internally multiplexed to $HRDATA_slv[31:0]$ read data bus, according to a linear Word aligned address decoding scheme. Namely, when the external AMBA AHB master device accesses through $HADDR[31:0]$ the address $0x00$, the $register0_in[31:0]$ port is returned in $HRDATA_slv[31:0]$ read data bus. For address $0x04$ the $register1_in[31:0]$ port is returned, for address $0x08$ the $register2_in[31:0]$ port is returned and so forth.

The user can arbitrarily drive the $register_i_in[31:0]$ input ports with Custom Interconnection Logic as shown in Figure 5-1. Consequently the returned values on $HRDATA$ read bus can be fully configured according to user needs. Table 5-1 describes the possible Read Data Path configurations.

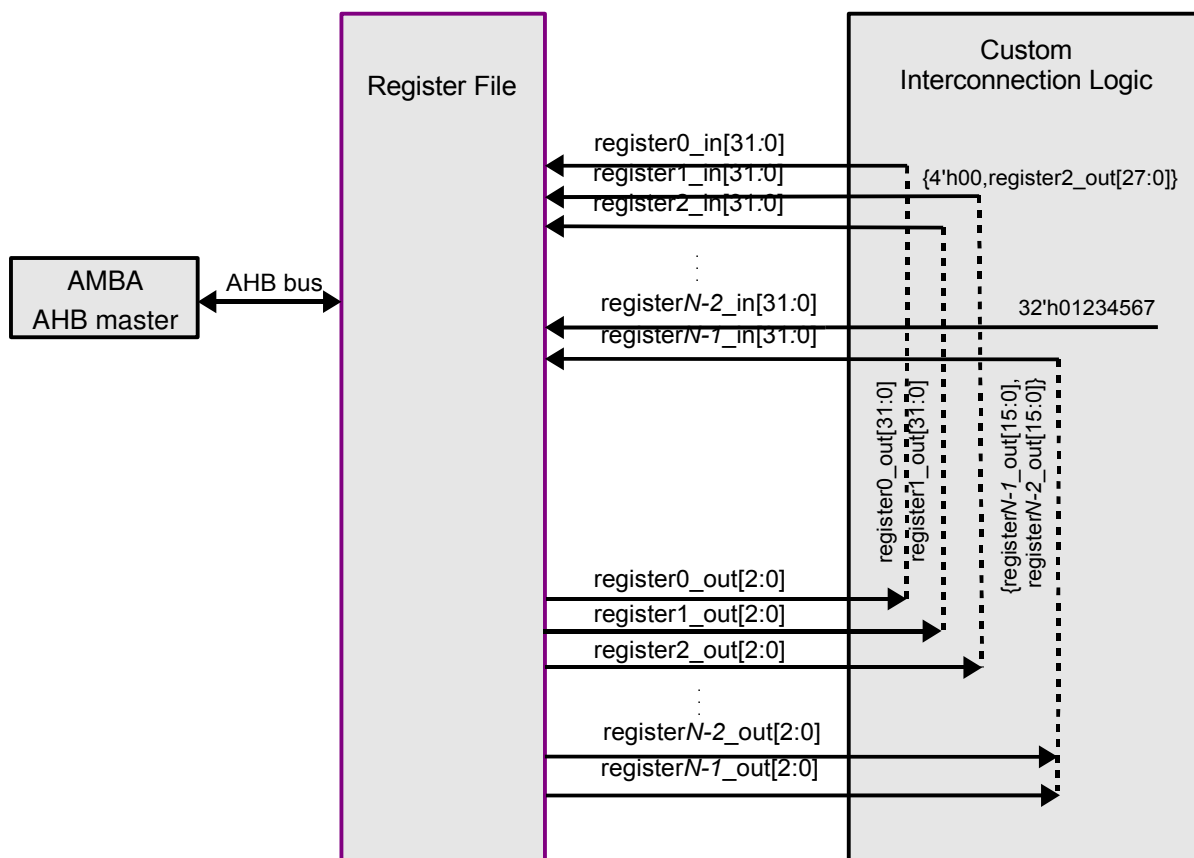


Figure 5-1 Interfacing Register File with an AMBA AHB master device and Custom Interconnection Logic

Table 5-1 Register File Read Data Path schemes

	READ DATA PATH SCHEME	DESCRIPTION
1	Linear Address- One-to-One Bits	register _i _out[31:0] output ports are bit-by-bit fully connected to register _i _in[31:0] input ports, namely register _i _out[0] is connected to register _i _in[0], register _i _out[1] is connected to register _i _in[1], and so forth. Consequently when register _i is read its actual contents are returned in HRDATA_slv bus.
2	Linear Address - Mixed Bits	Similar to <i>Linear Address- One-to-One Bits</i> scheme except that a arbitrary permutation can be applied on register _i _in to register _i _out connections.
3	Mixed Address – One-to-One Bits	Any register _i _out[31:0] output port can be arbitrarily connected to any register _i _in[31:0] input port. The bit interconnections rules are identical to <i>Linear Address- One-to-One Bits</i> scheme.
4	Mixed Address – Mixed Bits	Similar to <i>Mixed Address – One-to-One Bits</i> scheme except that bit interconnections rules are identical to <i>Linear Address - Mixed Bits</i> scheme. According to that scheme any bit of any register _i _out port can be connected to any bit of any register _i _in port.
5	Fully Custom	Corresponds to any combination of the previously described schemes. In addition to that, all or some of the register _i _in[31:0] bits can be hardwired to 1 or 0.

Figure 5-1 depicts a Fully Custom Read Data Path scheme. There is a *Linear address – One-to-One Bit* connection between register0_out and register0_in ports, a *Mixed Address – One-to-One* connection between register1_out and register2_in ports and Fully Custom connection scheme for registerN-2_out, registerN-1_out, registerN-2_in and registerN-1_in ports.

9 Deliverables

The package generated with *Registers for AMBA AHB* generator consists of the present document and source code files in Verilog HDL language. These files are listed in Table 6-1.

Table 6-1 *Registers for AMBA AHB* toolkit Deliverables

File	Description
AHBReg.v	<i>Register File</i> module
parameters.txt	<i>Register File</i> system parameters
TSi_AHBRegisters.pdf	The present document

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