

Think Silicon

VLSI Design & Consultancy

DATASHEET

**8b10b Encoder Decoder
Version 1.0**

1 Overview

The *8b10b Encoder Decoder* is a 8b10b encoder decoder web generator. The generated module performs DC balancing on transmission lines, providing that there are enough state transitions for clock recovery.

This 8b10b encoding scheme is used in many serial protocol standards including:

- PCI Express
- IEEE 1394b
- Serial ATA
- SAS
- Fiber Channel
- SSA
- Gigabit Ethernet (except for the twisted pair based 1000Base-T)
- InfiniBand
- XAUI
- Serial RapidIO
- DVI (Transition Minimized Differential Signaling)
- DVB Asynchronous Serial Interface (ASI)

The 8b10b encoding scheme is described on the U.S. Patent 4,486,739 (expired June 30, 2002) and is detailed on the paper by Franaszek and Widmer. The code represents a modified version of Chuck Benz, Hollis, NH original code.

2 Features

- 8b10b encoding/decoding according to U.S. Patent 4,486,739
- Independent 8b10b encoder and decoder blocks provide full duplex operation capability
- Fully synchronous operation

3 Architecture

3.1 Block Diagram

Figure 3-1 represents the basic functional block of the *8b10b Encoder Decoder* module. There are two blocks one for 8b10b encoding and one for 8b10b decoding. The *8b10b encoder* gets 8-bit frames and produces 10-bit frames according to the U.S. Patent 4,486,739 specifications. The *8b10b decoder* performs the exact opposite operation; gets 10-bit 8b10b encoded as inputs and reforms the original 8-bit data frames.

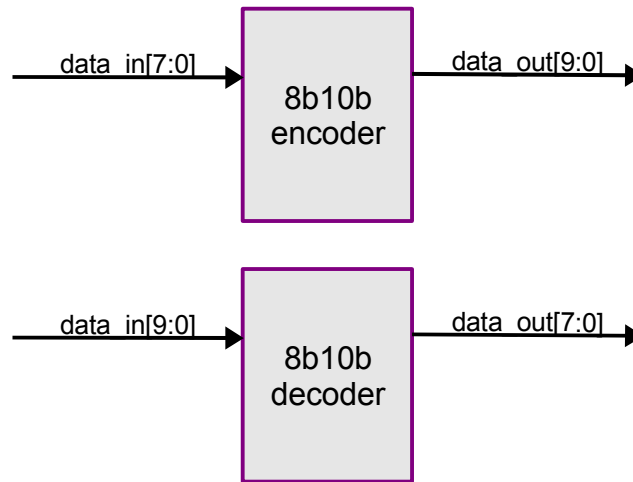


Figure 3-1 8b10b Encoder Decoder Block Diagram

3.2 Port Diagram

The 8b10b Encoder Decoder module Port Diagram is shown in Figure 3-2.

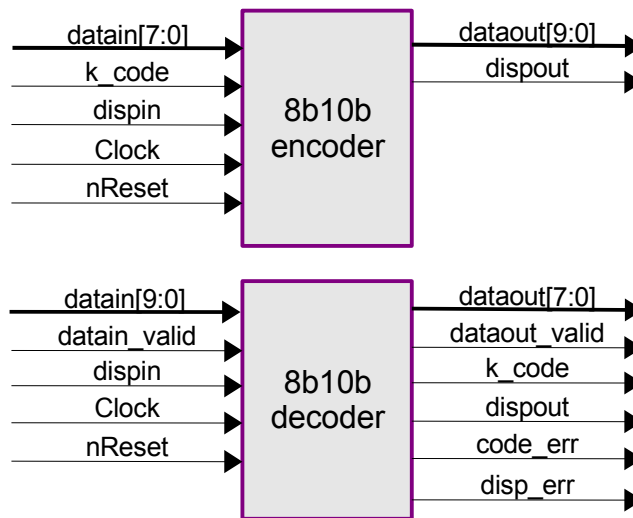


Figure 3-2 8b10b Encoder Decoder module Port Diagram

3.3 Port Interface

The port signals of 8b10b encoder are listed in Table 3-1.

Table 3-1 8b10b encoder Port Interface

PORT	TYPE	DESCRIPTION
Datain[7:0]	Input	8b data input frame
k_code	Input	Determines if data or k_code
dispin	Input	Requested disparity
Dataout[9:0]	Output	10b encoded data output frame

PORT	TYPE	DESCRIPTION
dispout	Output	Disparity
Clock	Input	Clock input (active high)
nReset	Input	Reset Input (active low)

The port signals of 8b10b decoder are listed in Table 3-2.

Table 3-2 8b10b decoder Port Interface

PORT	Direction	Description
datain[9:0]	Input	10b data input frame
dispin	Input	Disparity
dataout[7:0]	Output	8b decoded data
dataout_valid	Output	Asserted in case of valid data
k_code	Output	Asserted in case of k_code
code_err	Output	Asserted in case of invalid code
disp_err	Output	Asserted in case of invalid disparity
Clock	Input	Clock input (active high)
nReset	Input	Reset Input (active low)

4 Generator Usage

The 8b10b Encoder Decoder generator employs a graphical web user interface (GUI). In order to use the GUI you must sign-in Think Silicon Ltd web site. If already registered, click on *Sign-in* link in the upper, right side of the web page. Otherwise click on *Register* link first and follow the instructions. The 8b10b Encoder Decoder generator GUI page is shown in Figure 4-1. In order to generate the 8b10b Encoder Decoder module press the *Generate* button.

Twin Port Register based RAM

The screenshot shows a web-based GUI for generating a Twin Port Register based RAM. At the top, there are four tabs: 'Generator', 'Documentation', 'History', and 'License', with 'Generator' being the active tab. Below the tabs, there are four input fields: 'Address (locations)' with the value '256', 'Width (bits)' with the value '32', 'Synchronous read' with an unchecked checkbox, and 'Language' with a radio button selected for 'Verilog'. At the bottom left of the form area is a 'Generate' button.

5 Deliverables

The package generated with 8b10b Encoder Decoder consists of the present document and source code files in Verilog™¹ HDL language. The files are listed in Table 5-1.

Table 5-1 8b10b Encoder Decoder Deliverables

FILE	DESCRIPTION
./src/encode_8b_10b.v	8b10b encoder block
./src/tb_8b10b_enc.v	8b10b decoder block
./src/tb_8b10b_enc	8b10b Encoder Decoder testbench

¹ Verilog is a trademark of Cadence Design Automation. (<http://www.cadence.com>)

FILE	DESCRIPTION
parameters.txt	8b10b Encoder Decoder generation parameters
./doc/TSi_tpmems.pdf	The present document

6 Sample Data

Table 6-1 shows 8b10b encoding Sample Data.

Table 6-1 8b10b encoding Sample Data.

D:0 K:0	Datain:00	Dataout:1001110100	Disparity:0	NDA:00	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:01	Dataout:0111010100	Disparity:0	NDA:01	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:02	Dataout:1011010100	Disparity:0	NDA:02	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:03	Dataout:1100011011	Disparity:1	NDA:03	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:04	Dataout:1101010100	Disparity:0	NDA:04	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:05	Dataout:1010011011	Disparity:1	NDA:05	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:06	Dataout:0110011011	Disparity:1	NDA:06	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:07	Dataout:1110001011	Disparity:1	NDA:07	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:08	Dataout:1110010100	Disparity:0	NDA:08	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:09	Dataout:1001011011	Disparity:1	NDA:09	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:0a	Dataout:0101011011	Disparity:1	NDA:0a	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:0b	Dataout:1101001011	Disparity:1	NDA:0b	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:0c	Dataout:0011011011	Disparity:1	NDA:0c	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:0d	Dataout:1101001011	Disparity:1	NDA:0d	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:0e	Dataout:0111001011	Disparity:1	NDA:0e	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:0f	Dataout:0101110100	Disparity:0	NDA:0f	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:10	Dataout:0110110100	Disparity:0	NDA:10	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:11	Dataout:1000111011	Disparity:1	NDA:11	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:12	Dataout:0100111011	Disparity:1	NDA:12	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:13	Dataout:1100101011	Disparity:1	NDA:13	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:14	Dataout:0010111011	Disparity:1	NDA:14	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:15	Dataout:1010101011	Disparity:1	NDA:15	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:16	Dataout:0110101011	Disparity:1	NDA:16	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:17	Dataout:1110100100	Disparity:0	NDA:17	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:18	Dataout:1100110100	Disparity:0	NDA:18	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:19	Dataout:1001101011	Disparity:1	NDA:19	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:1a	Dataout:0101101011	Disparity:1	NDA:1a	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:1b	Dataout:1101100100	Disparity:0	NDA:1b	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:1c	Dataout:0011101011	Disparity:1	NDA:1c	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:1d	Dataout:1011001000	Disparity:0	NDA:1d	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:1e	Dataout:0111100100	Disparity:0	NDA:1e	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:1f	Dataout:1010110100	Disparity:0	NDA:1f	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:20	Dataout:1001111001	Disparity:1	NDA:20	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:21	Dataout:1110110011	Disparity:1	NDA:21	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:22	Dataout:1011011001	Disparity:1	NDA:22	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:23	Dataout:1100011001	Disparity:0	NDA:23	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:24	Dataout:1101011001	Disparity:1	NDA:24	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:25	Dataout:1010011001	Disparity:0	NDA:25	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:26	Dataout:0110011001	Disparity:0	NDA:26	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:27	Dataout:1110001001	Disparity:0	NDA:27	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:28	Dataout:1110011001	Disparity:1	NDA:28	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:29	Dataout:1001011001	Disparity:0	NDA:29	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:2a	Dataout:0101011001	Disparity:0	NDA:2a	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:2b	Dataout:1101001001	Disparity:0	NDA:2b	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:2c	Dataout:0011011001	Disparity:0	NDA:2c	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:2d	Dataout:1011001001	Disparity:0	NDA:2d	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:2e	Dataout:0111001001	Disparity:0	NDA:2e	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:2f	Dataout:0101111001	Disparity:1	NDA:2f	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:30	Dataout:0110111001	Disparity:1	NDA:30	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:31	Dataout:1000111001	Disparity:0	NDA:31	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:32	Dataout:0100111001	Disparity:0	NDA:32	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:33	Dataout:1100101001	Disparity:0	NDA:33	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:34	Dataout:0010111001	Disparity:0	NDA:34	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:35	Dataout:1010101001	Disparity:0	NDA:35	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:36	Dataout:0110101001	Disparity:0	NDA:36	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:37	Dataout:1110101001	Disparity:1	NDA:37	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:38	Dataout:1100111001	Disparity:1	NDA:38	NDISP:1	CERR:0	DERR:0	Ok
D:0 K:0	Datain:39	Dataout:1001101001	Disparity:0	NDA:39	NDISP:0	CERR:0	DERR:0	Ok
D:0 K:0	Datain:3a	Dataout:0101101001	Disparity:0	NDA:3a	NDISP:0	CERR:0	DERR:0	Ok


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D:1 K:0 Datain:f7 Dataout:0001011110 Disparity:1 NDATA:f7 NDISP:1 CERR:0 DERR:0 Ok
D:1 K:0 Datain:f8 Dataout:0011001110 Disparity:1 NDATA:f8 NDISP:1 CERR:0 DERR:0 Ok
D:1 K:0 Datain:f9 Dataout:1001100001 Disparity:0 NDATA:f9 NDISP:0 CERR:0 DERR:0 Ok
D:1 K:0 Datain:fa Dataout:0101100001 Disparity:0 NDATA:fa NDISP:0 CERR:0 DERR:0 Ok
D:1 K:0 Datain:fb Dataout:0010011110 Disparity:1 NDATA:fb NDISP:1 CERR:0 DERR:0 Ok
D:1 K:0 Datain:fc Dataout:0011100001 Disparity:0 NDATA:fc NDISP:0 CERR:0 DERR:0 Ok
D:1 K:0 Datain:fd Dataout:0100011110 Disparity:1 NDATA:fd NDISP:1 CERR:0 DERR:0 Ok
D:1 K:0 Datain:fe Dataout:1000011110 Disparity:1 NDATA:fe NDISP:1 CERR:0 DERR:0 Ok
D:1 K:0 Datain:ff Dataout:0101001110 Disparity:1 NDATA:ff NDISP:1 CERR:0 DERR:0 Ok
D:0 K:1 Datain:1c Dataout:0011110100 Disparity:0 NDATA:1c NDISP:0 CERR:0 DERR:0 Ok
D:0 K:1 Datain:3c Dataout:0011111001 Disparity:1 NDATA:3c NDISP:1 CERR:0 DERR:0 Ok
D:0 K:1 Datain:5c Dataout:0011110101 Disparity:1 NDATA:5c NDISP:1 CERR:0 DERR:0 Ok
D:0 K:1 Datain:7c Dataout:0011110011 Disparity:1 NDATA:7c NDISP:1 CERR:0 DERR:0 Ok
D:0 K:1 Datain:9c Dataout:0011110010 Disparity:0 NDATA:9c NDISP:0 CERR:0 DERR:0 Ok
D:0 K:1 Datain:bc Dataout:0011111010 Disparity:1 NDATA:bc NDISP:1 CERR:0 DERR:0 Ok
D:0 K:1 Datain:dc Dataout:0011110110 Disparity:1 NDATA:dc NDISP:1 CERR:0 DERR:0 Ok
D:0 K:1 Datain:fc Dataout:0011111000 Disparity:0 NDATA:fc NDISP:0 CERR:0 DERR:0 Ok
D:0 K:1 Datain:f7 Dataout:1110101000 Disparity:0 NDATA:f7 NDISP:0 CERR:0 DERR:0 Ok
D:0 K:1 Datain:fb Dataout:1101101000 Disparity:0 NDATA:fb NDISP:0 CERR:0 DERR:0 Ok
D:0 K:1 Datain:fd Dataout:1011101000 Disparity:0 NDATA:fd NDISP:0 CERR:0 DERR:0 Ok
D:0 K:1 Datain:fe Dataout:0111101000 Disparity:0 NDATA:fe NDISP:0 CERR:0 DERR:0 Ok
D:1 K:1 Datain:1c Dataout:1100001011 Disparity:1 NDATA:1c NDISP:1 CERR:0 DERR:0 Ok
D:1 K:1 Datain:3c Dataout:1100000110 Disparity:0 NDATA:3c NDISP:0 CERR:0 DERR:0 Ok
D:1 K:1 Datain:5c Dataout:1100001010 Disparity:0 NDATA:5c NDISP:0 CERR:0 DERR:0 Ok
D:1 K:1 Datain:7c Dataout:1100001100 Disparity:0 NDATA:7c NDISP:0 CERR:0 DERR:0 Ok
D:1 K:1 Datain:9c Dataout:1100001101 Disparity:1 NDATA:9c NDISP:1 CERR:0 DERR:0 Ok
D:1 K:1 Datain:bc Dataout:1100000101 Disparity:0 NDATA:bc NDISP:0 CERR:0 DERR:0 Ok
D:1 K:1 Datain:dc Dataout:1100001001 Disparity:0 NDATA:dc NDISP:0 CERR:0 DERR:0 Ok
D:1 K:1 Datain:fc Dataout:1100000111 Disparity:1 NDATA:fc NDISP:1 CERR:0 DERR:0 Ok
D:1 K:1 Datain:f7 Dataout:0001010111 Disparity:1 NDATA:f7 NDISP:1 CERR:0 DERR:0 Ok
D:1 K:1 Datain:fb Dataout:0010010111 Disparity:1 NDATA:fb NDISP:1 CERR:0 DERR:0 Ok
D:1 K:1 Datain:fd Dataout:0100010111 Disparity:1 NDATA:fd NDISP:1 CERR:0 DERR:0 Ok
D:1 K:1 Datain:fe Dataout:1000010111 Disparity:1 NDATA:fe NDISP:1 CERR:0 DERR:0 Ok
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