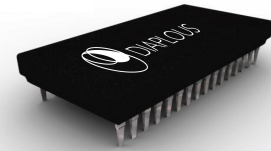


DIAPLOUS

COMPONENTS FOR VISUAL PERCEPTION



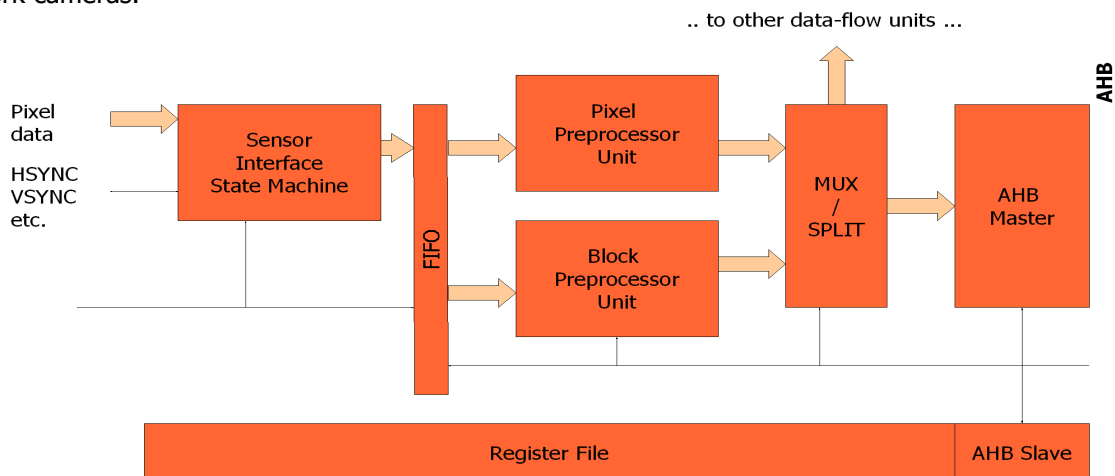
Sensor Interface with Image Preprocessor

Product Outline

SIIP: an Image Sensor Readout Module with Image Preprocessor

The DIAPLOUS Sensor Interface with Image Preprocessor (SIIP) module is an AMBA® 2 AHB™¹ compliant interface for connecting CMOS image sensors which includes preprocessing functions on the pixel-flow. This allows a major part of image processing algorithms to run directly during image capture without adding any load to the processor, to the bus or to other units of an image processing system.

It handles all required synchronization with the sensor chip and reads data into a FIFO memory for clock decoupling. The raw and processed pixel data can then be transferred over the AHB bus to on-chip or external memory for further processing. This makes the SIIP an ideal solution for applications where a large amount of pixel and block level image processing is required like machine vision, surveillance and high-speed network cameras.



Sensor Interface State Machine: Assembles the Bayer pattern data received from the sensor port to true color information (24-bits per pixel) and feeds them to the FIFO block. It can also perform conversion to other pixel color formats (YUV, RGB565, Monochrome).

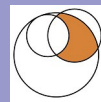
FIFO: A memory block that decouples the clocks of the sensor and the AMBA bus. It stores multiple pixel rows before they are used by the two preprocessor units.

AHB Master / Slave: An AHB master device that transfers pixels in burst mode to a memory device via the AHB bus, and an AHB slave for configuration and control of the SIIP core via the Register File.

Pixel Preprocessor Unit: Performs operations to extract pixel-specific features like color match, luminance and chroma thresholds, color or intensity quantization etc.

Block Preprocessor Unit: Performs operations on small blocks of pixels, yielding pixel features like gradient, texture etc as well as block-level features like small corners and lines, sub-sampling etc.

¹ AMBA® is a registered trademark of ARM Limited. AHB™ is a trademark of ARM Limited.



Features:

- AHB2.0 master device for connecting to a CMOS sensor.
- Configurable True Color Resolution (typical 1024x768 - Bayer pattern: 2048x1536, can grow up to 8Mpixels depending on available on-chip memory and required speed)
- Supports Single 32-bit transactions on the Bus as well as Burst 16-word transfers
- Image and feature data pushed on user programmable memory regions.
- Supports color (bayer pattern, RGB565, YUV422) sensors with parallel data output in sensor master mode.
- Supports conversion to RGB, YUV, Monochrome
- Includes Pixel Feature Extraction operations
 - Thresholds
 - Color Match (eg. for skin detection)
 - Quantization
 - Palette conversion
- Includes Block Level Feature Extraction
 - Gradients (for edge detection)
 - Texture matching
 - Discovery of Corner and Line Structures
 - Average (for resolution reduction)
 - Simple Configurable Filters
- Can provide direct output to another pixel-flow unit for further processing
- Frame start/end signals
- Enable/Disable Capability
- Two-wire interface for sensor programming
- Sensor configuration is using I2C interface (e.g. the I2C code from Opencores, available with modifications to attach on the AHB bus).

Target Applications:

- Industrial Vision Cameras
- Surveillance Systems
- Interactive Games and Education
- Robotics
- IP cameras etc.



Distributor & Sales:

Think Silicon
VLSI Design & Consultancy

Think Silicon Ltd.

Patras Science Park
Rion Ahaia 26504
Greece

<http://www.think-silicon.com>

info@think-silicon.com

Tel: +30 2610 911543

Interfaces:

- 32bit AHB Master
- Sensor Port (Sensor signals: Sync, Pixel Data).
- Status Bits, Control Bits through AHB
- Pixel-flow Output

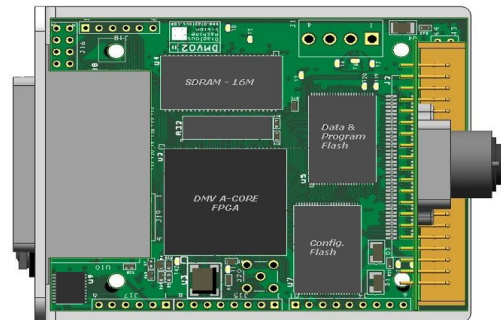
Software:

- C library for: Frame Capture, Sensor Programming, Region of Interest / Skip / Bin, Sensor programming, Preprocessor Configuration etc.
- Example Firmware Application that detects persons by doing skin extraction, filtering and blob detection
- PC based application for quick setup and view of captured images through Ethernet 10/100 (live video) or RS232 (still images).

Note: The C library is for the embedded firmware running on the evaluation FPGA chip. The PC applications are two: one on Windows XP and the other on Linux.

Status: Working FPGA Implementation.

Evaluation:



Development board including:

- FPGA with RISC Core, Ethernet 10/100 MAC, Sensor Interface, I2C, Memory Interface
- Memories (SDRAM & Flash)
- Ethernet Phy & Connector
- 3Mpixel Color Image Sensor

More info:

DIAPLOUS
COMPONENTS FOR VISUAL PERCEPTION

Diaplous Ltd.

Epistimoniko Parko Patras
Platani, 26500
Greece

<http://www.diaplous.com>

info@diaplous.com

Tel: +30 6945 934 408